

Docket No.: W&B-INF-1859

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : JOHANN PFEIFFER ET AL.  
Filed : CONCURRENTLY HEREWITH  
Title : CIRCUIT AND METHOD FOR WRITING AND READING DATA  
FROM A DYNAMIC MEMORY CIRCUIT

INFORMATION DISCLOSURE STATEMENT

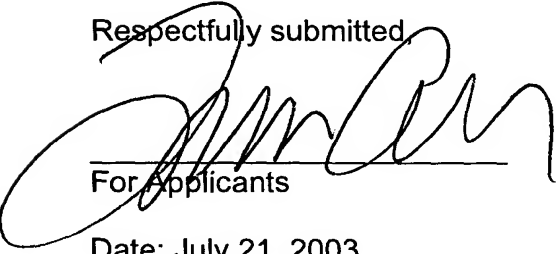
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

Sugibayashi, T. et al.: "A 30-ns 256-Mb DRAM with a Multidivided Array Structure",  
IEEE Journal of Solid-State Circuits, Vol. 28, No. 11, November 1993, pp. 1092-  
1098.

Respectfully submitted,

  
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For Applicants

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Date: July 21, 2003

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<b>FORM PTO-1449 (SUBSTITUTE)</b>  U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  <b>INFORMATION DISCLOSURE          STATEMENT BY APPLICANT</b> (37 CFR 1.98(b))				Attorney Docket No.: W&B-INF-1859 Appl. No.: _____  Applicant: JOHANN PFEIFFER ET AL.  Filing Date: July 21, 2003 Group Art Unit: _____			
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EXAMINER INITIALS	PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
A						
B						
C						
D						
E						
F						
G						
H						
I						

FOREIGN PATENT DOCUMENT							
DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO	
J							
K							
L							
M							
N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)	
	Sugibayashi, T. et al.: "A 30-ns 256-Mb DRAM with a Multidivided Array Structure", IEEE Journal of Solid-State Circuits, Vol. 28, No. 11, November 1993, pp. 1092-1098

<b>EXAMINER</b>	<b>DATE CONSIDERED</b>
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<b>EXAMINER:</b> Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
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